Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION**

1. **OFFSET**
2. **– INPUT**
3. **+ INPUT**
4. **V –**

**6 N/C**

**7 V +**

**8 OFFSET ADJ**

**7 6**

**8**

**1**

**2 3**

**4**

**.070”**

**.060”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0045” X .0045”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .060” X .070” DATE: 8/25/21**

**MFG: HARRIS THICKNESS .019” P/N: HA0-2705-6**

**DG 10.1.2**

#### Rev B, 7/19/02